DATA SHEET

Bluetooth™

UAA3559UH
Bluetooth RF transceiver

Objective specification

2003 Jul 04

Philips
Semiconductors

PHILIPS

Bluetooth RF transceiver UAA3559UH

FEATURES

- Low cost solution for a Bluetooth™(1) radio
- Fully integrated receiver with high sensitivity
- Integrated low phase noise VCO
- Dedicated Bluetooth Phase-Locked Loop (PLL) synthesizer
- Transmitter preamplifier with programmable output power of up to 9 dBm
- 3-line serial interface bus
- Low current consumption from 3.0 V supply.

APPLICATIONS

2402 to 2480 MHz Bluetooth radio transmission and reception in the Industrial Scientific and Medical (ISM) band conforming to the "*Bluetooth Specification Version 1.1*."

GENERAL DESCRIPTION

The UAA3559HN BiCMOS device is a low-power, highly integrated circuit. It features a fully integrated receiver for demodulating the output signal from an external antenna filter, an integrated VCO, a synthesizer to implement Bluetooth channel frequencies, and a transmitter preamplifier. The output power of the transmitter preamplifier can be programmed in eight steps from −7.5 dBm to +9 dBm (typical) and drives either an antenna via an external switch diode or an external power amplifier.

(1) The Bluetooth trademarks are owned by Bluetooth SIG, Inc., U.S.A. and licensed to Koninklijke Philips Electronics N.V.

The synthesizer comprises a reference divider, main divider with prescaler, and a phase comparator. The division ratios of both dividers are programmed by control signals on a 3-wire bus. The main divider accepts a frequency range of 2402 to 2481 MHz from the internal VCO. The reference divider accepts either a 12 or 13 MHz signal from an external crystal oscillator. The outputs of both dividers are compared by a phase comparator. A charge-pump in the comparator produces a current pulse output whenever a phase error occurs. The current pulse output signal controls and phase locks the VCO frequency. The charge-pump current (phase comparator gain) is set to 4 mA.

After the synthesizer is programmed, it is activated about 200 μs before the required channel time slot to allow time for the VCO to lock to the channel frequency. The synthesizer is then deactivated just before the desired slot to allow open loop modulation of the VCO in transmit mode. The synthesizer is also deactivated just before the desired slot in receive mode. This is required to reduce power consumption and allows adjustment of the VCO by an internal carrier follower circuit to maintain an accurate IF.

The IC is designed to operate from 3.0 V nominal supplies. Separate power pads are provided for different parts of the circuit. The ground pads should be connected together externally to prevent large, potentially harmful, currents flowing through the IC. All supply pads must be at the same potential.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UAA3559UH	–	bare die; on foil; die dimensions 2.3 × 2.1 mm	–

QUICK REFERENCE DATA

V_{CC} = 3.0 V; T_{amb} = 25 °C; characteristics for which only a typical value is given are indicative unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.7	3.0	3.4	V
$I_{CC(RX)(guard)}$	receiver supply current during RX guard space	VCO = on, PLL = closed	–	20	–	mA
$I_{CC(RX)}$	receiver supply current	VCO = on; PLL = open; receiver = on	–	40	48	mA
$I_{CC(TX)(guard)}$	transmitter supply current during TX guard space	VCO = on; PLL = closed	–	17	–	mA
$I_{CC(TX)}$	transmitter supply current	VCO = on; TX preamplifier = on; bits [12:10] = 100	–	33	40	mA
$I_{CC(pd)}$	supply current in Power-down mode		–	5	30	µA
f_{LO}	synthesized Local Oscillator (LO) frequency		2402	–	2480	MHz
$f_{i(xtal)}$	crystal reference input frequency	reference divider ratio				
		12	–	12	–	MHz
		13	–	13	–	MHz
$f_{ph(comp)}$	phase comparator frequency		–	1	–	MHz
T_{amb}	ambient temperature		–30	+25	+85	°C

BLOCK DIAGRAM

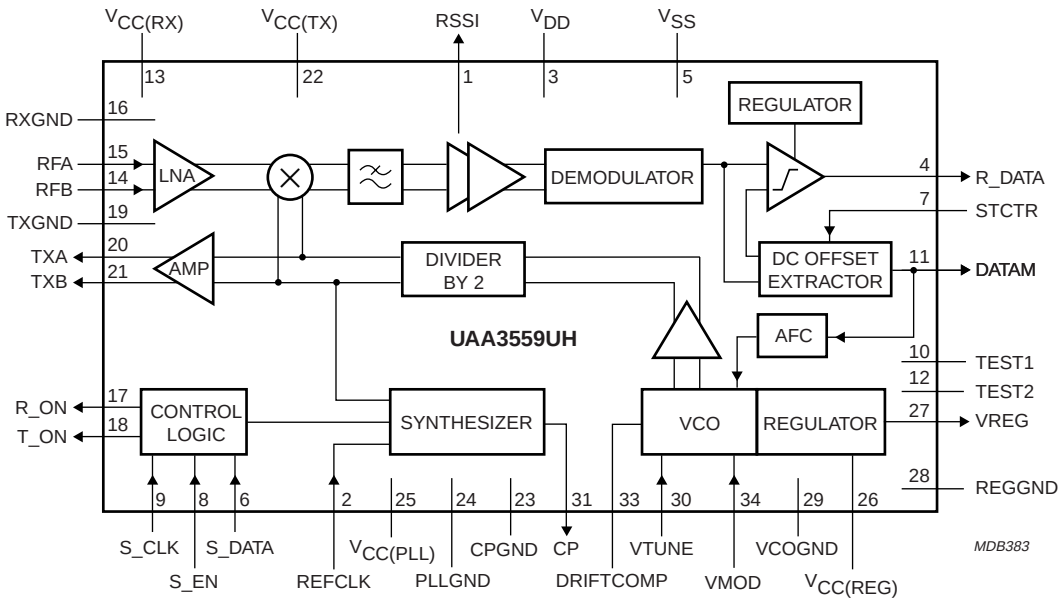

Fig.1 Block diagram.

PINNING

SYMBOL	PAD	DESCRIPTION
RSSI	1	received signal strength intensity voltage output
REFCLK	2	reference frequency input
V_{DD}	3	logic supply voltage
R_DATA	4	digital received data output
V_{SS}	5	logic ground
S_DATA	6	3-wire bus data signal input
STCTR	7	receiver DC extractor and TX preamplifier timing control input
S_EN	8	3-wire bus enable signal input
S_CLK	9	3-wire bus clock signal input
TEST1	10	test pad 1; do not connect
DATAM	11	receive data analog decision voltage output
TEST2	12	test pad 2; do not connect
$V_{CC(RX)}$	13	receiver supply voltage
RFB	14	received signal input B
RFA	15	received signal input A
RXGND	16	receiver ground
R_ON	17	receiver PIN diode control digital output
T_ON	18	transmitter PIN diode control digital output
TXGND	19	transmitter ground
TXA	20	transmitted signal output A
TXB	21	transmitted signal output B
$V_{CC(TX)}$	22	transmitter supply voltage
CPGND	23	charge-pump ground
PLLGND	24	VCO ground
$V_{CC(PLL)}$	25	PLL supply voltage
$V_{CC(REG)}$	26	regulator supply voltage
VREG	27	regulator output voltage
REGGND	28	regulator ground
VCOGND	29	synthesizer ground
VTUNE	30	VCO tuning input
CP	31	charge-pump output
n.c.	32	not connected
DRIFTCOMP	33	VCO drift compensation
VMOD	34	modulation input
GND	die pad	ground

FUNCTIONAL DESCRIPTION

Transmit chain

VCO; BUFFER AND DIVIDER

The VCO has a fully integrated tank circuit with on-chip inductors, and an on-chip regulator which minimizes any frequency disturbances caused by V_{CC} variations. The VCO regulator requires a decoupling capacitor to be connected to pad VREG. The VCO operates at twice the Bluetooth frequency.

The VCO signal is buffered and fed into a divide-by-two circuit to produce the required Local Oscillator (LO) frequencies for either transmit (TX) mode or receive (RX) mode. The large difference between the transmitter and VCO frequencies reduces transmitter to oscillator coupling problems.

The output of the divide-by-two circuit drives the main divider prescaler in the synthesizer and also drives the TX preamplifier in TX mode, or the RX LO buffer in RX mode. The high isolation between the VCO buffer and the main divider ensures that only very small frequency changes occur when the TX preamplifier or the RX section are turned on. In the TX mode, the VCO is directly modulated with GFSK data at pad VMOD.

TRANSMIT PREAMPLIFIER

The TX preamplifier gain is programmable in seven steps of up to 4 dB. It can either amplify the RF signal up to a level of 9 dBm (typical), or attenuate the RF signal to −7.5 dBm (typical), see Table 5.

The output of the TX preamplifier at pads TXA and TXB can directly drive an antenna via a PIN diode switch and band filter for Bluetooth power class 2 and 3 applications.

The type of TX preamplifier load can affect the frequency of the VCO when the preamplifier powers up. This ‘pulling’ effect can be counteracted by changing the time at which the preamplifier powers up, and is implemented by selecting one of two possible ramp-up modes: ramp-up mode 0 or ramp-up mode 1. In ramp-up mode 0, the preamplifier powers up on the rising edge of STCTR. In ramp-up mode 1, the preamplifier powers up on the falling edge of STCTR; see Table 3 and timing diagrams Figs 2 and 3.

Synthesizer

MAIN DIVIDER

The main divider is clocked by the RF signal from the VCO via the divide-by-two circuit at a frequency in the range 2402 to 2481 MHz.

The divider ratio is programmable to any value in the range 2304 to 2559 inclusive; see Table 6.

REFERENCE DIVIDER

The reference divider is clocked by the reference signal at either 12 or 13 MHz via pad REFCLK. The divider ratio is programmable to 12 or 13. The circuit operates in the range 150 to 500 mV (RMS); see Table 4.

PHASE COMPARATOR

The outputs of both the main divider and reference divider drive a phase comparator. Its charge-pump circuit outputs current pulses at pad CP. The CP signal connects to pad VTUNE to complete the PLL, which controls and phase locks the VCO frequency. The duration of a current pulse is equal to the difference in time between the arrival of the leading edges of both dividers outputs. If the leading edge from the main divider arrives first, the charge-pump sinks current. If the leading edge from the reference divider arrives first, the charge-pump sources current. The CP signal current can be integrated by connecting an external RC loop filter to pad VTUNE as shown in Fig.5.

An internal drift compensation circuit maintains the VCO frequency when the synthesizer is deactivated during open loop modulation. It requires an external capacitor to be connected to pad DRIFTCOMP.

Additional internal circuits ensure that the gain of the phase comparator remains linear even for small phase errors.

Serial programming bus

The IC is programmed by a simple 3-line unidirectional serial bus comprising data (S_DATA), clock (S_CLK) and enable (S_EN). The serial data is loaded as a burst that is framed by S_EN. The programming clock edges and corresponding data bits are ignored until S_EN goes LOW. The program data is read directly by the main divider when S_EN goes HIGH. Signals S_DATA and S_EN should change value on the falling edge of S_CLK. When inactive, S_CLK should be held LOW.

The internal register stores only the last 32 bits of data that are serially clocked into the IC. Additional leading bits are ignored, and no check is made on the number of clock pulses received. The allocation of data bits in the IC register is shown in Table 1; the first bit entered is bit 31, the last bit is bit 0.

Signal S_EN also controls the operation of the PLL by either activating or deactivating the internal synthesizer. The PLL opens for a brief interval after the falling edge of S_EN.

Receiver

The receiver is a fully integrated Bluetooth RF and IF strip, and demodulator. It provides all of the channel filtering required over the Bluetooth band, and provides either an analog or a digital signal at output R_DATA. The very few off-chip components required should not require any trim adjustment.

The receiver input signal is fed from the RF antenna, via either a band filter or an antenna switch to pads RFA and RFB. A representation of the instantaneous received signal strength is output at pad RSSI.

The local oscillator frequency is half the VCO frequency and must be tuned to 1 MHz above the received channel frequency to produce a 1 MHz IF. A DC offset extractor circuit obtains the DC component of the demodulated analog signal. A comparator compares the extracted DC with the demodulated analog signal to produce a digital stream signal at pad R_DATA.

The level of extracted DC at the comparator is carefully adjusted by the occurrence and duration of signal STCTR. During the alternating ones and zeroes of the trailer code, pad STCTR should normally be set HIGH. The baseband must ensure that STCTR is synchronized with the received data.

There are two modes for extracting the DC component from the demodulated signal: mode 0 and mode 1. Both modes use two methods for DC extraction using a MinMax circuit and an RC integrating circuit. The MinMax circuit quickly determines the average DC component from the maximum and minimum swings of the demodulated signal. The remaining DC is extracted by one or two RC circuits. The MinMax circuit is enabled following the 16 μs delay after the falling edge of S_EN. When pad STCTR goes HIGH, the MinMax circuit is disabled and the RC circuit is enabled. In mode 0, an RC circuit with a fast time constant is enabled. In mode 1 an RC circuit with a slow time constant is enabled. When STCTR goes LOW, in mode 0, the fast time constant RC circuit is disabled and a slow time constant RC circuit is enabled.

In mode 1, the slow time constant RC circuit remains enabled. The slow time constant RC circuit in either mode is disabled on the rising edge of the second S_EN pulse. The RC resistors for modes 0 and 1 are internal; an external capacitor has to be connected to pad DATAM.

The timing of these actions is shown in Fig.4.

Operating mode

The IC timing is controlled by signal S_EN. In TX mode, after the register is programmed via S_DATA, the transmitter is activated on the falling edge of STCTR. The rising edge of S_EN activates the PLL, closes the loop and powers up the VCO regulator. The falling edge of STCTR is emulated by the output signal on pad T_ON which can be used to activate an external power amplifier or antenna switch. On the falling edge of this first S_EN pulse, the loop opens, unless bit 9 (PLL) is set; see Figs 2 and 3, and Table 1.

In RX mode (bit TRX = 1), the receiver is activated on the falling edge of S_EN and is ready to demodulate data 16 μs later. The falling edge of S_EN is emulated by the output signal on pad R_ON which is suitable for driving an external receiver PIN diode.

At the end of a time slot period, a second S_EN pulse is required to power-down the receiver or transmitter chain and synthesizer.

Power-down mode

In Power-down mode, current consumption is reduced to below 60 μA. Pads R_ON and T_ON are in 3-state output mode. The IC enters Power-down mode on the falling edge of each S_EN pulse that is not preceded by an S_CLK signal edge.

Register description

Table 1 Register bit allocation

REGISTER BIT(1)	VALUE(2)	NAME
31	1	–
30	0	–
29	1	–
28 to 26	0	–
25	1	–
24 to 23	0	–
22	–	AFC
21 to 20	1	–
19	–	TX ramp-up mode
18	–	DC extractor mode
17	0	–
16	1	–
15	0	–
14	–	REF1
13	–	REF0
12 to 10	–	TX output power
9	–	PLL
8	–	TRX mode
7 to 0	–	main divider programming

Notes

1. In normal operation, 32 bits are programmed into the register; bit 31 is read in first and bit 0 last.
2. Those bits allocated with values are reserved for test purposes and must be programmed with this value.

Table 2 Description of register bits

BIT	FUNCTION	DESCRIPTION
22	AFC	Automatic Frequency Control. AFC is used to follow transmitter carrier in RX mode. 0 = AFC OFF and 1 = AFC ON
19	TX ramp-up mode	See Table 3
18	DC extractor mode	DC extractor mode programming. 0 = mode 0; MinMax - fast RC followed by slow RC time constants; 1 = mode 1, MinMax - slow RC time constants; see timing diagrams in Fig.4.
14 to 13	REF1 and REF0	These bits define the reference divider ratio of the synthesizer; see Table 4
12 to 10	TX output power	These bits set the TX preamplifier output power; see Table 5.
9	PLL	PLL mode. 1 = PLL remains ON while the VCO is on; 0 = the PLL is opened at the start of the active slot period.
8	TRX mode	Transmit or receive mode. 1 = RX mode selected; 0 = TX mode selected.
7 to 0	main divider programming	The main divider ratio is equal to 2304 + n where the binary code for n is given by bits 7 to 0 with bit 7 as the MSB; see Table 6.

Table 3 TX ramp-up sequence

TX RAMP-UP MODE BIT 19		RESULT
LOGIC 0	LOGIC 1	
S_EN rising edge	STCTR rising edge	TX preamplifier bias stage on
STCTR rising edge	STCTR falling edge	TX preamplifier output stage on
STCTR falling edge	STCTR falling edge	pad T_ON HIGH
S_EN rising edge	S_EN rising edge	PLL ON (closed)
S_EN falling edge	S_EN falling edge	PLL OFF (open; bit 9 = 0)
S_EN reset rising edge	S_EN reset rising edge	PLL OFF (closed; bit 9 = 1)
S_EN reset falling edge	S_EN reset rising edge	TX preamplifier bias stage OFF
S_EN reset rising edge	S_EN reset rising edge	TX preamplifier output stage OFF
S_EN reset rising edge	S_EN reset rising edge	pad T_ON LOW

Table 4 Reference divider programming

BIT 14	BIT 13	REFERENCE DIVIDER RATIO	REFERENCE FREQUENCY INPUT (MHz)
0	0	12	12
1	0	13	13

Table 5 Transmitter preamplifier output power programming

BIT 12	BIT 11	BIT 10	TX OUTPUT POWER, TYPICAL TARGET (dBm)
0	0	0	–7.5
0	0	1	–4.5
0	1	0	–0.5
0	1	1	+1.5
1	0	0	+4.5
1	0	1	+8
1	1	0	+9
1	1	1	+9

Table 6 Main divider programming (example)

BIT								MAIN DIVIDER RATIO	SYNTHESIZED FREQUENCY (MHz)	CHANNEL
7	6	5	4	3	2	1	0			
Binary equivalent of n								2304 + n	1.0 × (2304 + n)	
0	1	1	0	0	0	1	0	2402	2402	transmit channel 0
0	1	1	0	0	0	1	1	2403	2403	receive channel 0
1	0	1	1	0	0	0	0	2480	2480	transmit channel 78
1	0	1	1	0	0	0	1	2481	2481	receive channel 78

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	−0.3	+3.6	V
V_n	voltage on any pad	0	V_{CC}	V
$P_{i(max)}$	maximum power at receiver input	–	0	dBm
T_{stg}	storage temperature	−55	+125	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	−30	+85	°C

Note

1. All ground pads must be connected together externally on the printed circuit board to prevent a large current flowing through the die.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

All pads withstand 1000 V HBM and 50 V MM ESD test in accordance with *"EIA/JESD22-A114-B Class1 (June 2002)"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; exposed die-pad soldered on a 4 layer FR4 PCB	30	K/W

CHARACTERISTICS

V_{CC} = 3.0 V; T_{amb} = 25 °C; Δf = 160 kHz; characteristics for which only a typical value is given are not tested unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		2.7	3.0	3.4	V
$I_{CC(RX)(guard)}$	receiver supply current during RX guard space	VCO = on PLL = closed	–	20	–	mA
$I_{CC(RX)}$	receiver supply current	receiver = on; VCO = on; PLL = open	–	40	48	mA
$I_{CC(TX)(guard)}$	transmitter supply current during TX guard space	VCO = on; PLL = closed	–	17	–	mA
$I_{CC(TX)}$	transmitter supply current	TX preamplifier = on; VCO = on; bits [12:10] = 100	–	33	40	mA
$I_{CC(pd)}$	supply current in Power-down mode		–	5	30	µA
Synthesizer main divider						
D/D_{main}	main divider ratio		2402	–	2481	
$f_{o(RF)}$	RF output frequency		2402	–	2480	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Synthesizer reference divider input						
$f_{i(xtal)}$	crystal reference input frequency	reference divider ratio				
		12	–	12	–	MHz
		13	–	13	–	MHz
$V_{i(xtal)(rms)}$	sinusoidal input signal level (RMS value)		0.15	–	2	V
R_i	resistive part of the input impedance	f_{ref} = 13 MHz	–	2	–	kΩ
C_i	capacitive part of the input impedance		–	2.5	–	pF
Phase detector						
$f_{ph(comp)}$	phase comparator frequency		–	1	–	MHz
Charge-pump output						
I_L	charge-pump leakage	$V_{CP} = 0.5V_{CC}$; note 1	–	–	5	nA
I_o	charge-pump output current	$V_{CP} = 0.5V_{CC}$; note 1	–	3.5	–	mA
VCO						
f_{LO}	synthesized Local Oscillator (LO) frequency	T_{amb} = –30 to +85 °C; note 2	2402	–	2481	MHz
$\Delta f_{VCO(VTUNE)}$	frequency variation with voltage on pad VTUNE	defined at LO frequency; $0.3 < V_{CP} < (V_{CC} - 0.3)$	–	120	–	MHz/V
$\Delta f_{(slope)(l)}$	tuning slope low band	note 3	–	110	–	MHz/V
$\Delta f_{(slope)(h)}$	tuning slope high band	note 3	–	110	–	MHz/V
$\Delta f_{VCO(mod)}$	frequency variation with modulation input	defined at LO frequency; $V_{VMOD(DC)}$ = 0.9 V	0.8	1.0	1.2	MHz/V
TX preamplifier						
P_o	output power	T_{amb} = –30 to +85 °C; note 2				
		bits [12:10] = 111	–	9	–	dBm
		bits [12:10] = 110	–	9	–	dBm
		bits [12:10] = 101	–	8	–	dBm
		bits [12:10] = 100	–	4.5	7.5	dBm
		bits [12:10] = 011	–	1.5	–	dBm
		bits [12:10] = 010	–	–0.5	–	dBm
		bits [12:10] = 001	–	–4.5	–	dBm
		bits [12:10] = 000	–	–7.5	–	dBm
$P_{o(step)}$	output power step	T_{amb} = –30 to +85 °C; notes 2 and 4	–	3	–	dB
R_o	resistive part of parallel output impedance	balanced; at 2450 MHz	–	tbf	–	Ω
C_o	capacitive part of parallel output impedance	balanced; at 2450 MHz	–	tbf	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$VCO_{(feedthru)}$	VCO signal feedthrough level at TX output	referenced to P_o at 2450 MHz; note 2	–	–20	–	dBc
C/N	carrier-to-noise ratio at TX output	carrier offset = 500 kHz	–	–107	–89	dBc/Hz
		carrier offset = 2500 kHz	–	–126	–	dBc/Hz
Receiver section; notes 5 and 6						
$f_{i(RF)}$	RF input frequency		2402	–	2480	MHz
$V_{o(RSSI)}$	RSSI output voltage	monotonic over range –86 to –36 dBm				
		with –36 dBm at RF input	–	1.6	1.8	V
		with –86 dBm at RF input	–	0.3	0.5	V
t_{wake}	wake-up time between receiver power-up and correct RSSI output	no external capacitor on pad RSSI	–	8	25	µs
$\Delta P_{i(sens)}$	input sensitivity	BER ≤ 10^{-3}; with TX carrier frequency offset up to ±115 kHz for T_{amb} = –30 to +85 °C; note 2	–	–85	–73	dBm
$P_{i(max)}$	maximum useable input level	BER ≤ 10^{-3}; note 2	–23	–	–	dBm
α_{im}	intermodulation rejection	BER ≤ 10^{-3}; desired channel = –67 dBm; interfering frequency at 5 and 10 channels away from desired channel; note 2	–	34	–	dBc
α_{co}	co-channel rejection	BER ≤ 10^{-3}; desired channel = –63 dBm; note 2	–11	–10	–	dBc
$\alpha_{(n\pm1)}$	adjacent channel rejection (n ± 1)	BER ≤ 10^{-3}; desired channel = –63 dBm; level of adjacent channel referenced to level of desired channel; note 2	0	3	–	dBc
$\alpha_{(n-2)}$	bi-adjacent channel rejection (n – 2)	BER ≤ 10^{-3}; desired channel = –63 dBm; level of bi-adjacent channel referenced to level of desired channel; note 2	30	33	–	dBc
$IR_{(n+2)}$	image frequency rejection (n + 2)	BER ≤ 10^{-3}; desired channel = –63 dBm; level of image frequency referenced to level of desired channel; note 2	9	12	–	dBc
$IR_{(n+3)}$	adjacent image frequency rejection (n + 3)	BER ≤ 10^{-3}; desired channel = –70 dBm; level of adjacent image frequency referenced to level of desired channel; note 2	20	23	–	dBc
$\alpha_{(n-\geq3)(n+\geq4)}$	rejection with more than three channels separation 0 to (n – 3) and (n + 4) to 78	BER ≤ 10^{-3}; desired channel = –70 dBm; level of adjacent channel referenced to level of desired channel; note 2	40	43	–	dBc

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{OOB(block)}$	rejection of an out-of-band blocking signal	BER ≤ 10^{-3}; desired channel = –70 dBm; level of CW interferer referenced to level of desired channel; range: 2 to 3 GHz; note 2	40	43	–	dBc
$P_{LO(feedthru)}$	local oscillator feedthrough level	f_{VCO} 2450 MHz	–	–80	–	dBm
R_i	RF resistive part of the parallel input impedance	balanced; at 2450 MHz	–	76	–	Ω
C_i	RF capacitive part of the parallel input impedance	balanced; at 2450 MHz	–	0.6	–	pF
Interface logic input and output signal levels; pads S_DATA, S_CLK, S_EN, T_ON, R_ON, R_DATA and STCTR						
V_{IH}	HIGH-level input voltage	note 7;	1.4	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–	–	0.4	V
V_{OH}	HIGH-level output voltage	for R_DATA output; note 7	2.4	2.5	–	V
V_{OL}	LOW-level output voltage	for R_DATA output; note 7	–	–	0.4	V
$I_{i(bias)}$	input bias current	logic 1 or logic 0	–5	–	+5	µA
$I_{source(R\_ON)}$, $I_{source(T\_ON)}$	output current source capability on pads R_ON and T_ON		–	4	–	mA
f_{S_CLK}	3-wire bus frequency		–	–	7	MHz
t_{S_EN}	S_EN pulse duration	to enable Power-down mode	2	–	–	µs
		to lock the PLL and calibrate	140	160	–	µs

Notes

1. Suitable for a typical locking time of 160 µs including filter calibration.
2. Measured and guaranteed only on the Philips evaluation board, including printed-circuit board and balun filter; not including PIN diode or band filter loss. Measured on a packaged die.
3. The slope for G_{avg} is evaluated with V_{VTUNE}: $\Delta f_{(slope)} = \frac{\Delta f}{\Delta V_{VTUNE}}$
4. TX preamplifier power steps form a monotonic sequence.
5. BER measurement conditions are described in *"Bluetooth BER method"*.
6. All receiver section parameters are measured at the receiver balun input, and a 3 dB loss is assumed for the antenna path. The values expressed in dBc refer to the level of the interfering signal and are positive for interfering signal levels higher than the desired signal level.
7. The output of pad R_DATA is designed to interface with pad R_DATA of the Philips baseband IC.

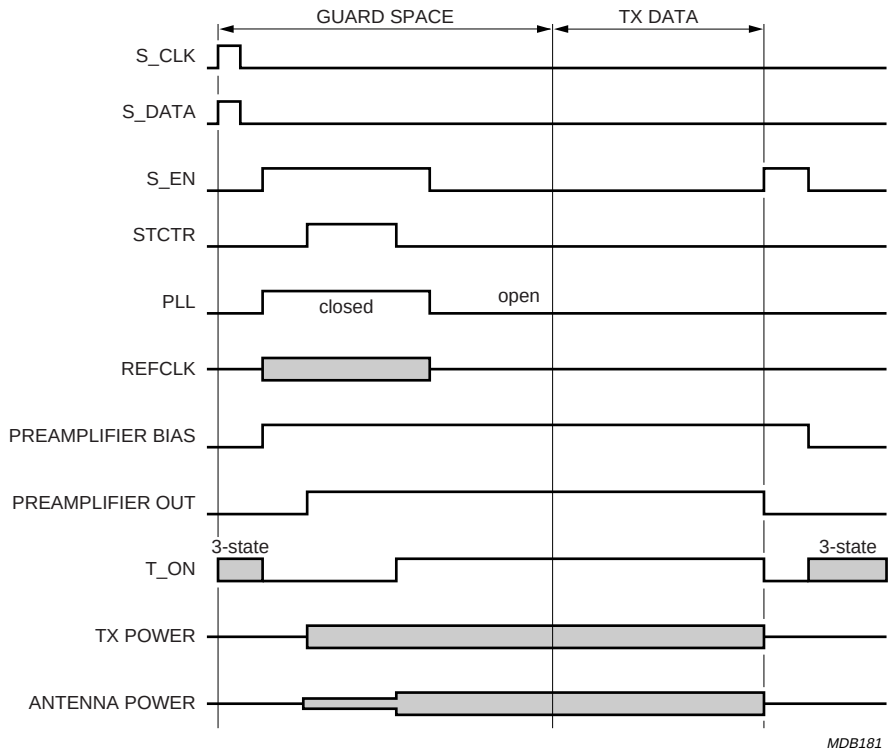

Fig.2 TX slot timing, ramp-up mode 0.

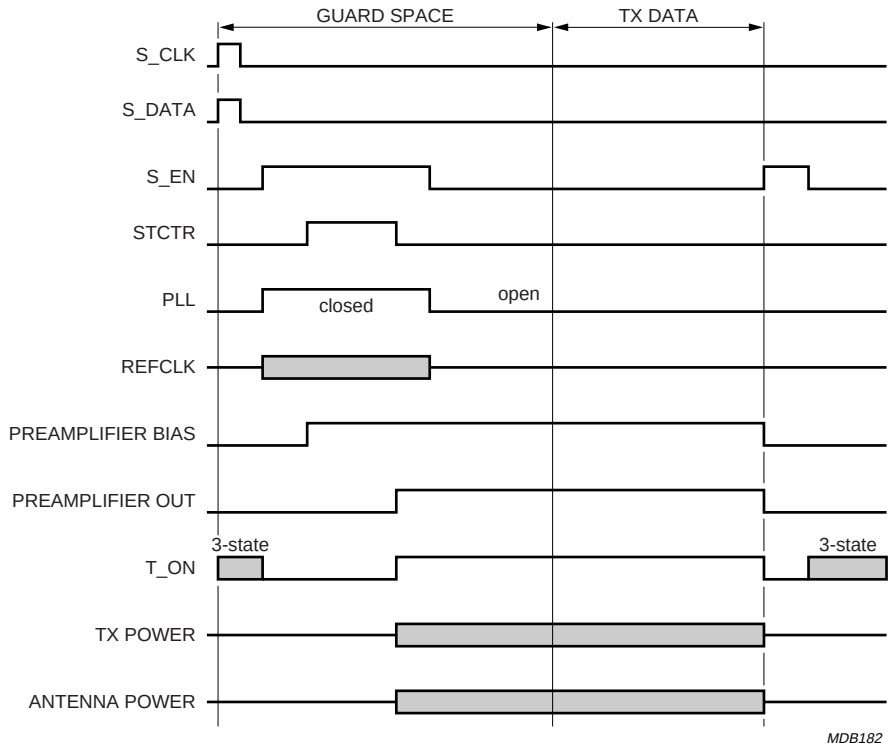

Fig.3 TX slot timing, ramp-up mode 1.

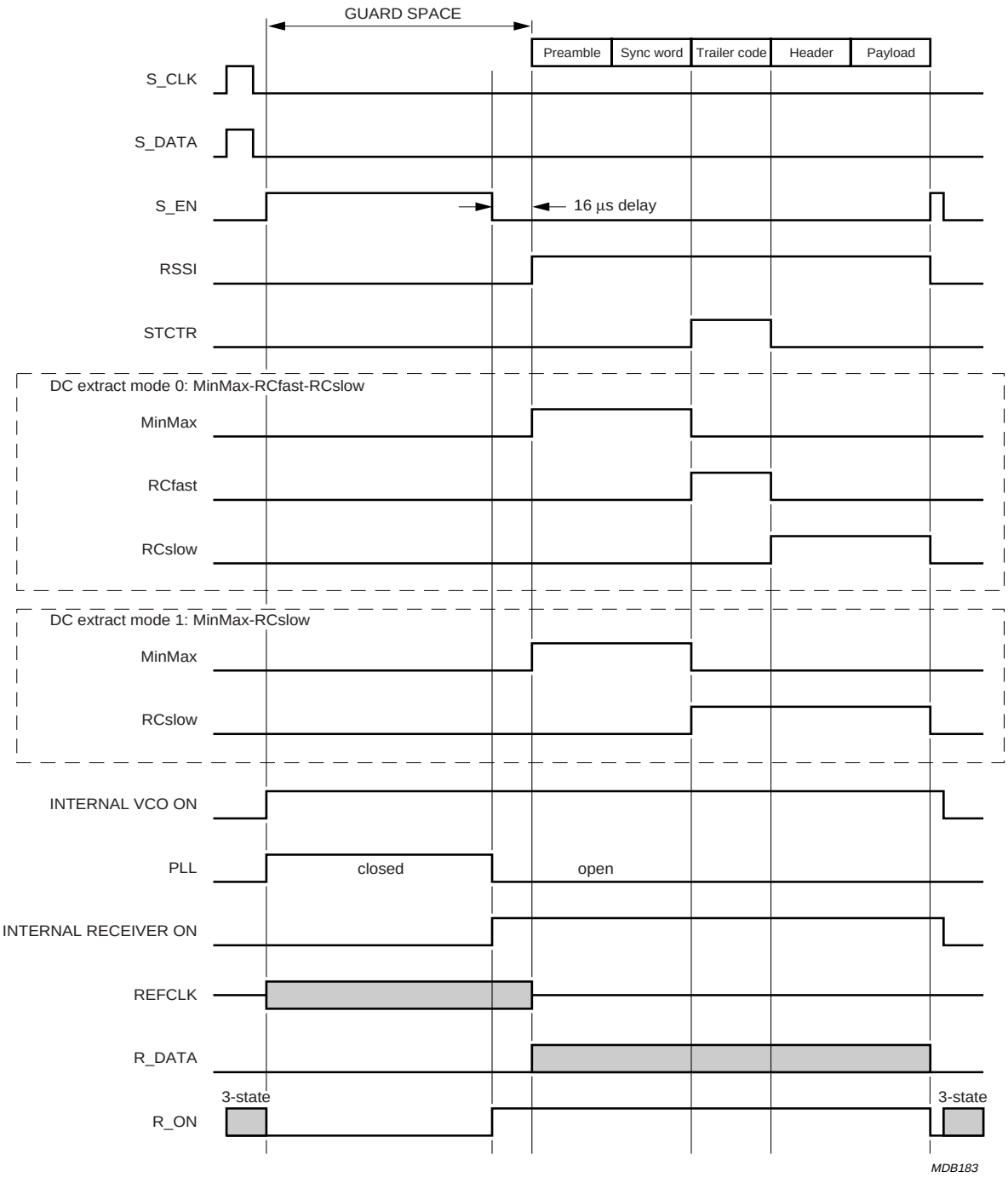

Fig.4 RX slot timing.

APPLICATION INFORMATION

The schematic shows a typical application diagram. Component values depend on the application. Two time constants are set by an external capacitor, their values are given and are suitable for most applications:

- The value of C_{DATAM} is chosen to optimize the time constants of the AFC, and DC extractor modes 0 and 1. The typical value of C_{DATAM} for AFC is 10 nF. If AFC is not used, C_{DATAM} adjusts the RC time constant of DC extractor modes 0 and 1.
- The value of $C_{DRIFTCOMP}$ is chosen to set the time constant of the VCO drift compensation. The typical value is 6.8 nF.

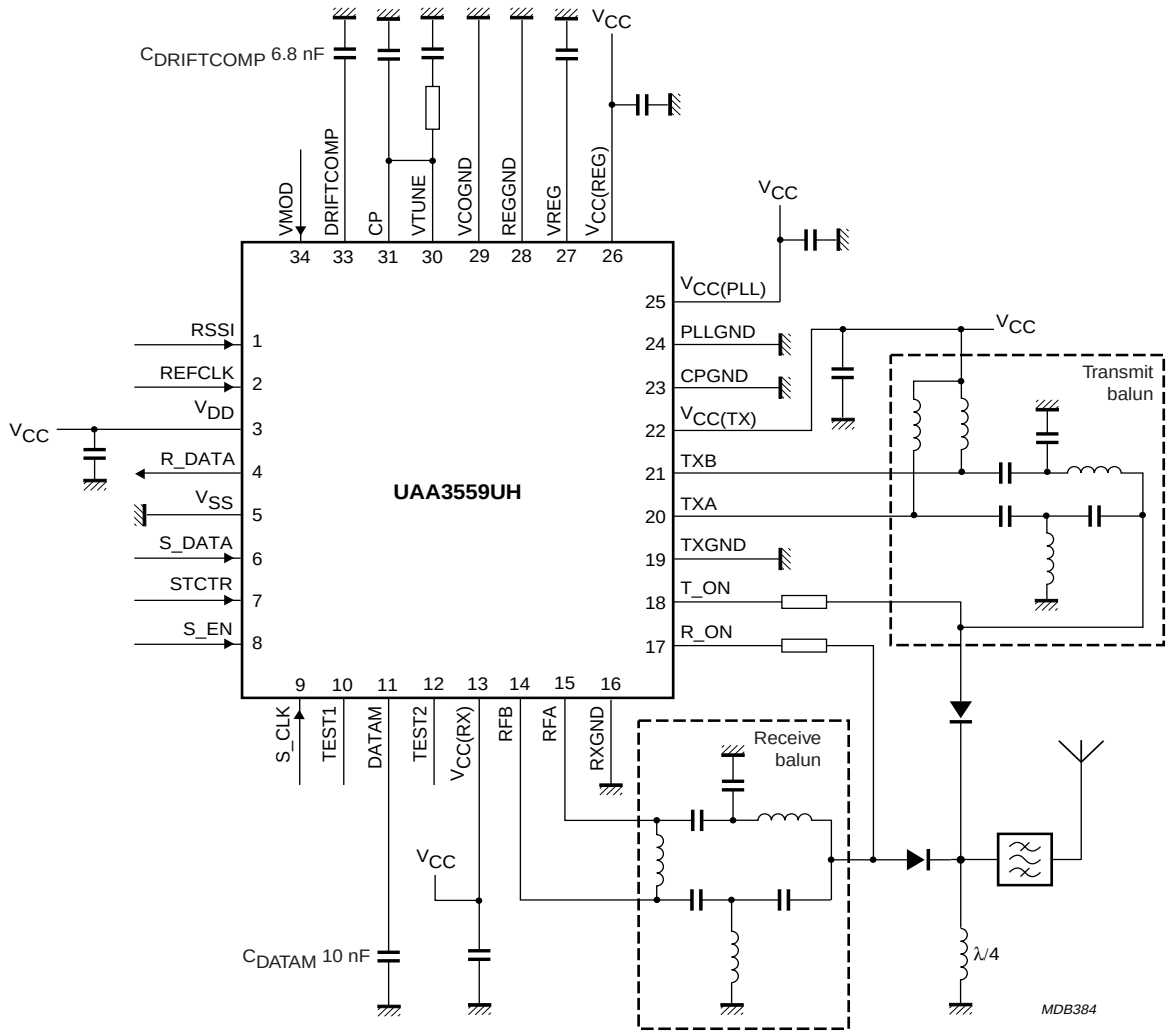

Fig.5 Application diagram.

BONDING PAD LOCATIONS

All x/y coordinates represent the position of the centre of the pad (in μm) with respect to the origin (x/y = 0/0) of the die; see Fig. x). The size of all square pads is 90 μm x 90 μm. The size of other pad shapes are less than 80 μm x 80 μm.

SYMBOL	PAD	COORDINATES	
		x	y
RSSI	1	−1103.7	+759.3
REFCLK	2	−1103.7	+594.3
V_{DD}	3	−1103.7	+285.3
R_DATA	4	−1103.7	+109.4
V_{SS}	5	−1103.7	−79.3
S_DATA	6	−1103.7	−232.7
STCTR	7	−1103.7	−550.1
S_EN	8	−1103.7	−737.7
S_CLK	9	−884.3	−1001.3
TEST1	10	−705.5	−1001.3
DATAM	11	−372.1	−1001.3
TEST2	12	−170.2	−1001.3
$V_{CC(RX)}$	13	+374.0	−1001.3
RFB	14	+619.3	−1001.3
RFA	15	+775.8	−1001.3
RXGND	16	+951.7	−1001.3
R_ON	17	+1104.3	−809.1
T_ON	18	+1104.3	−642.4
TXGND	19	+1104.3	−485.8
TXA	20	+1104.3	−192.6
TXB	21	+1104.3	−28.6
$V_{CC(TX)}$	22	+1104.3	+238.5
CPGND	23	+1104.3	+503.5
PLLGND	24	+1104.3	+692.4
$V_{CC(PLL)}$	25	+1104.3	+860.0
$V_{CC(REG)}$	26	+939.2	+1006.7
VREG	27	+759.8	+1006.7
REGGND	28	+587.8	+1006.7
VCOGND	29	+313.4	+1006.7
VTUNE	30	+28.6	+1006.7
CP	31	−167.4	+1006.7
n.c.	32	−532.9	+1006.7
DRIFTCOMP	33	−712.8	+1006.7
VMOD	34	−889.8	+1006.7

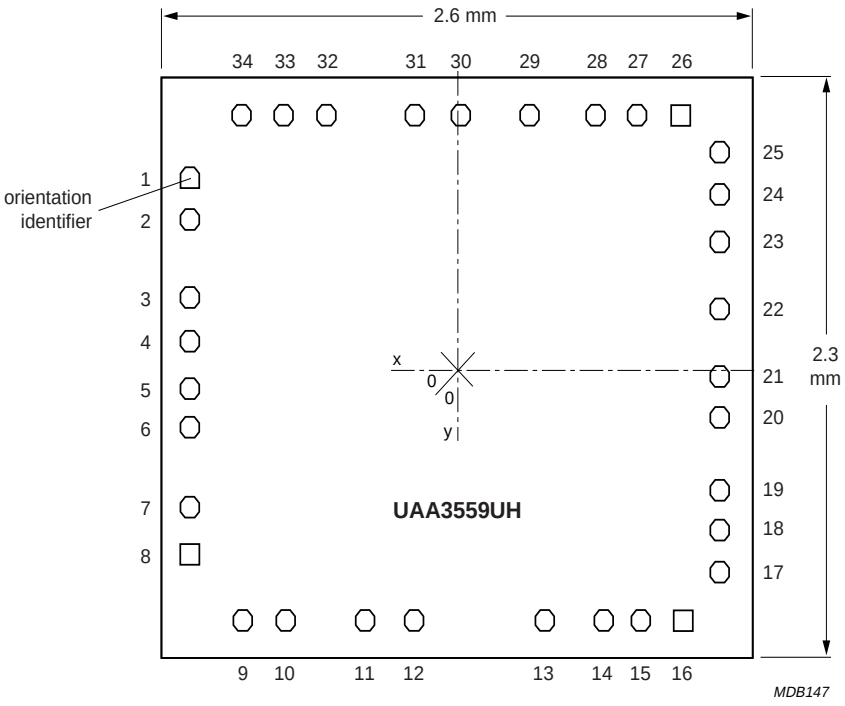

Fig.6 Bonding pad locations.

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Printed in The Netherlands 403506/01/pp22 Date of release: 2003 Jul 04 Document order number: 9397 750 10912

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